BEE 332 Devices and circuits II
Spring 2017
Lab 2: Single-stage BJT amplifiers*

1 Objectives

The objectives of this experiment are to observe the operating characteristics of the four basic single-stage BJT amplifier circuits shown here in figures 1 through 4: common emitter, common emitter with bypassed emitter resistor, common collector (also called an emitter follower), and common base.

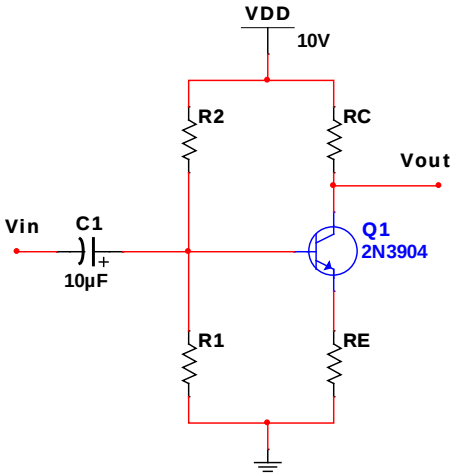

Figure 1. Common emitter.

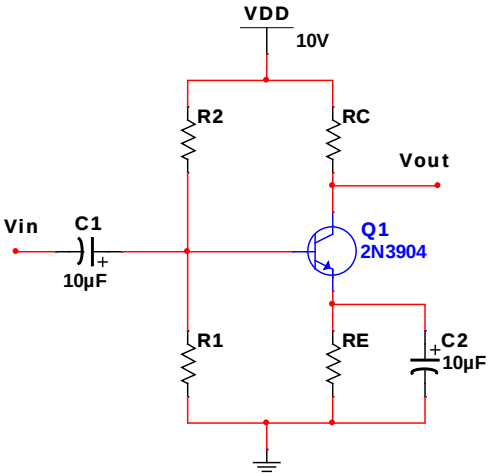

Figure 2. Common emitter with bypassed emitter resistor.

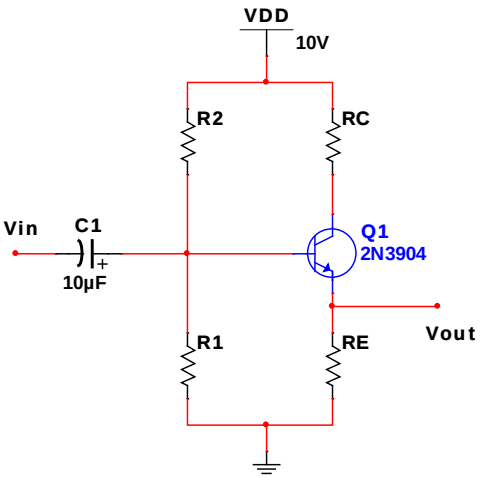

Figure 3. Common collector (emitter follower).

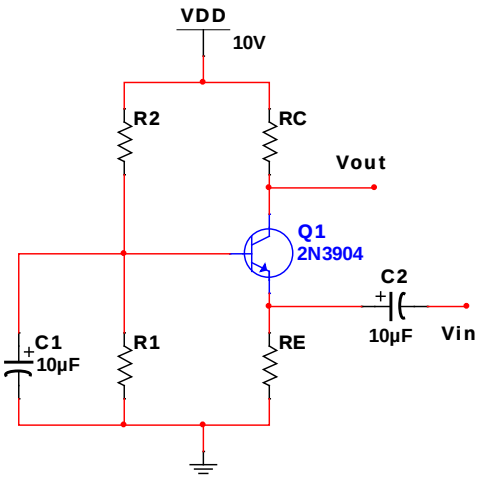

Figure 4. Common base.

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* This lab was originally created by R. B. Darling at UW Seattle and has been updated by R. Yotter, T. Chen and N. Hamilton.

You will both simulate and build each of these circuits, taking measurements to determine the gain and the clipping and 3 dB cutoff points to see how they behave and how they compare.

2 Using a BJT as an amplifier

There are two parts to using a transistor as amplifier, biasing it into the forward active region and choosing the circuit configuration appropriate to the application.

The transistor is a three terminal device. Used as two-port network, one terminal can be the output, one can be the input and the one that's left must be common to both the input and output ports.

For a transistor to work as an amplifier, the circuit must be designed so that any change in the input will cause a change in IB, causing a change βF times that in IC. Thus, two rules apply to single stage BJT amplifiers: The base can never be an output, and the collector can never be an input.

With these rules, there are three fundamental BJT amplifier stages:

1. Common emitter (CE) where the input is on the base and the output on the collector,
2. Common base (CB) where the input is on the emitter and the output on the collector, and
3. Common collector (CC), also known as an emitter-follower (EF) where the input is on the base and the output is on the emitter.

This laboratory experiment will examine the characteristics of each of these three fundamental amplifier configurations.

3 The Q point: Biasing an NPN transistor

Biasing a BJT into the forward-active region of operation is the first required step in creating an amplifier stage. Once the BJT is properly biased it can be used as an amplifier by injecting the input into one terminal and extracting the output from another.

Biasing is done by establishing a Q point, meaning the "quiescent" or "quiet" point, usually in the forward active region, establishing DC voltages at the transistor's terminals to forward bias the base-emitter junction and reverse bias the base-collector junction. At this point, the transistor has been turned on but there's no signal applied.

Choosing a bias point depends on both the transistor and the application, but troubleshooting malfunctioning transistor amplifier circuits can almost always be accomplished by simply checking the biasing with a DMM or oscilloscope to insure that the voltages on each terminal are in the correct relationship to each other. Use this procedure to become acquainted with what a properly biased BJT "looks like" with a DMM or oscilloscope so that you can then recognize an improperly biased one later on.

3.1 Setup

Figure 5 shows the basic bias network. You will choose the resistor values as you progress through the measurement part of this procedure

R1, R2, RE and RC should all be 5% 1/4 W resistors values to be chosen. Q1 is a 2N3904 NPN BJT.

Begin by establishing +10.0 V and Gnd (ground) power supply rails on your breadboard.

Keep the power supply turned OFF, and only turn it ON briefly to check a voltage value while you are assembling this circuit. This is a good practice to get into the habit of doing. Drop the power while you are making changes to it. While plugging and unplugging parts on the breadboard, you can very easily subject the devices to over-voltage or over-current which could destroy them. Dropping the power assures that this will not occur.

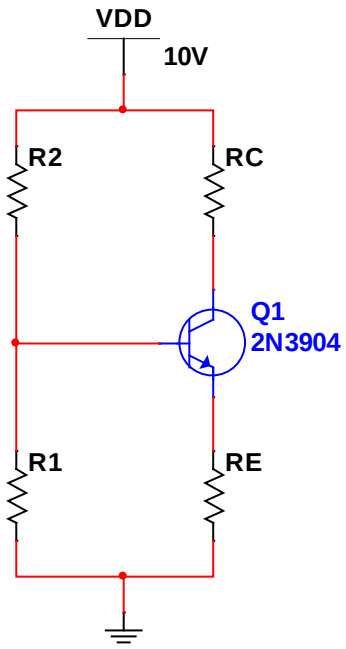

Figure 5. Bias circuit.

3.2 Measurements

3.2.1 Establish the base voltage

The first step in biasing a transistor is establishing the base voltage.

This will be done through the resistor voltage divider chain of R1 and R2.

1. Design a voltage divider chain of R1 and R2 that puts the base voltage at approximately 1.5 V, relative to ground. Pick values for R1 and R2 that give a voltage division ratio of around 5.67:1 (to give 1.5 V from the 10 V power rail) and which runs about 150 µA through it. Please show your calculations.
2. The expected base current used by Q1 will be around 10 µA or less, so making the current flow through R1 and R2 about 15 times this value should make the voltage between R1 and R2 nearly independent of the level of base current.
3. Locate these resistors, plug them into the breadboard, and briefly power up the circuit to verify that the node between R1 and R2 is at approximately 1.5 V. Record your measured voltage in your lab notebook.

3.2.2 Choose RE

With the base voltage at about 1.5 V, the emitter voltage will then be approximately 0.7 V less than this, or at about 0.8 V.

4. Pick a value for RE so that the 0.8 V across RE produces a current flow of about 0.8 mA, which is to be the emitter current of Q1.
5. Plug Q1 into the breadboard, connecting its base to the node between R1 and R2, and connecting its emitter to the Gnd rail through the RE that you have chosen. Leave the collector unconnected for the moment, as shown in Figure 6.
6. Power up the circuit and measure the base and emitter voltages, recording the results in your lab notebook.

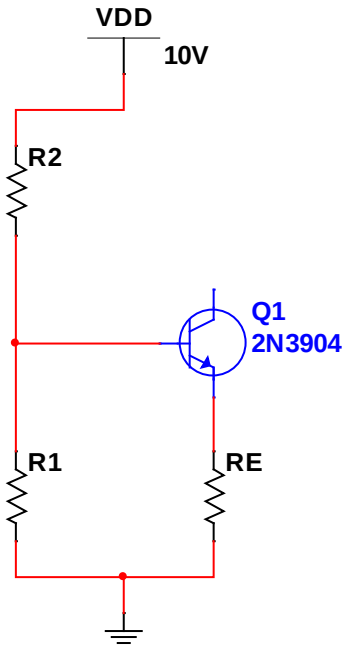

Figure 6. Collector disconnected.

Your measured values should be lower than the values you designed for because Q1 is not yet acting like a transistor. With the collector open-circuited, the base-emitter junction behaves only as a diode, which turns on and puts RE and R1 almost in parallel.

The heavier value of base current in this case pulls the base voltage down below your design value.

7. Power the circuit OFF, connect the collector of Q1 to the +10 V power rail as shown in figure 7.
8. Briefly power the circuit ON, measure the base and emitter voltages again, and record these in your lab notebook.

Since the emitter current is now being supplied by the collector connection, the base current is much lower now, and the base voltage should be closer to your design value of around 1.5 V.

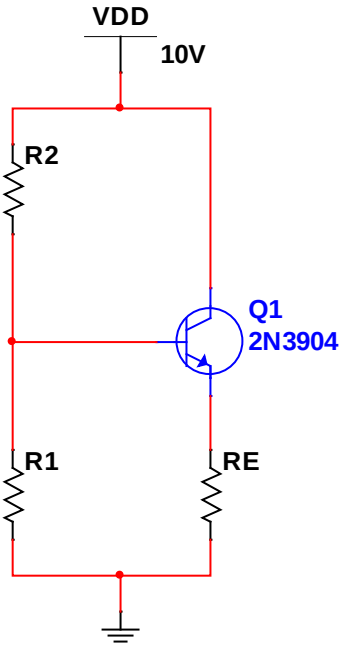

Figure 7. Collector tied to VDD.

3.2.3 Choose RC

Assuming that the emitter and collector currents are now both about 0.8 mA,

9. Choose a value for RC to drop the collector voltage down to about +6 V, relative to the Gnd rail.

10. Turn the power supply OFF, insert your value of RC into the collector branch, completing the bias circuit in figure 5.
11. Briefly turn the power back ON and measure the emitter, base, and collector voltages of Q1, each relative to the Gnd rail. Record all three of these in your lab notebook.

At this point, you should have a properly biased-up NPN BJT, ready to turn into an amplifier.

3.2.4 Summary

Transistor amplification requires that the BJT be operated in the forward active region, which is what the biasing exercise is attempting to produce. Forward active operation requires a forward-biased base-emitter junction and a reverse-biased base-collector junction.

Review your measured values of emitter, base, and collector voltages and verify that this is correct for forward-biasing an NPN BJT.

If in the future you encounter a BJT which is not behaving properly as an amplifier, first check it to insure that it is biased up properly so that its terminal voltages have the same voltage relationships as the BJT in this procedure. The ability to rapidly troubleshoot transistor biasing problems will put you way ahead in the game of building amplifiers!

Save this circuit. It will be used in the next four procedures.

3.3 Questions

From your measured values of VE, VB, and VC,

1. Calculate the current flowing through each resistor, and the emitter, base, and collector currents for the transistor.
2. Verify that the terminal currents for the transistor sum to zero as required by Kirchoff's Current Law.
3. Calculate the value of β for the transistor in this bias state.
4. For a forward-active NPN BJT, order the emitter, base, and collector voltages in increasing order.
5. For a forward-active PNP BJT, order the emitter, base, and collector voltages in increasing order.

4 Common emitter amplifier

In the next four procedures, the biased-up NPN BJT will be employed in four different types of single-stage amplifiers. These next four procedures will all be similar; as you move through them, take note of the differences between the behaviors of the different amplifier configurations.

In the common emitter configuration, shown in figure 8 (same as figure 1), the input is applied to the base through C1, a 10 µF electrolytic capacitor, and the output is taken at the collector. As Vin changes, it has the effect of slightly wiggling VB, causing a change in IC.

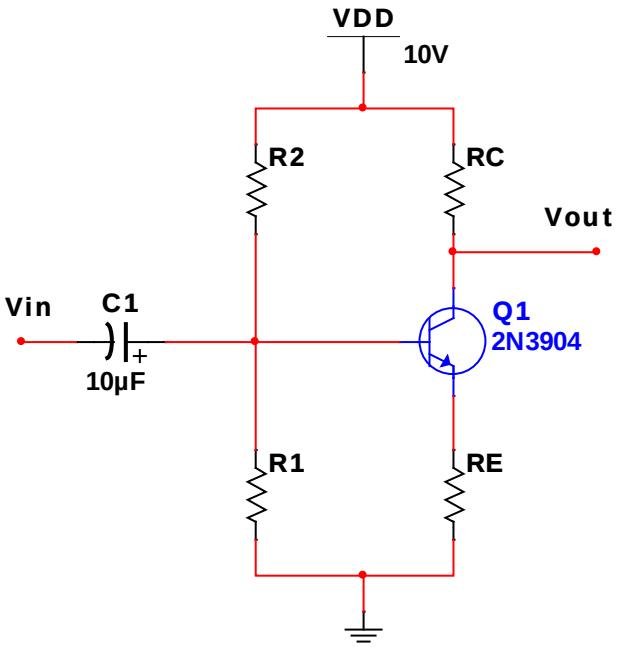

Figure 8. Common emitter amplifier.

4.1 Simulation

Create a simulation using SPICE or Multisim of this circuit and copy and paste your schematic into your report.

4.1.1 Gain

1. Capture a screenshot of Vin and Vout from your simulation with Vin = 1.0 Vpp sine wave at 1.0 kHz with suitable cursors.
2. Calculate the voltage gain, Av = $\frac{|Vout|}{|Vin|}$, of this amplifier as the ratio of the amplitude of Vout to amplitude of Vin.

4.1.2 Clipping

3. Increase Vin until Vout begins clipping one peak or the other. Capture a screenshot with suitable cursors.
4. Continue increasing Vin until Vout begins clipping on both peaks. Capture a screenshot with suitable cursors.

4.1.3 Bandwidth

A key performance parameter for an amplifier is its bandwidth, or how high in frequency it can maintain the voltage gain that it exhibits at 1 kHz.

5. Reset Vin = 1.0 Vpp sine wave at 1.0 kHz.

6. Increase the frequency, holding the input amplitude constant, until Av has dropped by 3 dB. This is known as the cutoff frequency and is the point at which Vout has dropped to sqrt(1/2) = 70% of its value at 1.0 kHz. Capture a screenshot with suitable cursors.

4.2 Setup

Starting from the forward-biased NPN circuit,

1. Add capacitor C1 = 10 µF electrolytic capacitor as shown in figure 8 (same as figure 1).
2. Set Vin = 1.0 Vpp sine wave at 1.0 kHz.
3. Configure the oscilloscope with Vin on channel 1 and Vout on channel 2 using DC coupling.
4. Turn the DC power supply ON to energize the circuit.
5. Adjust the oscilloscope to give a clear display of Vin and Vout with appropriate scales and on-screen measurements.

Vout should be centered about a DC level of about 6 V and should have a much larger amplitude than Vin. If so, then congratulations on building your first amplifier.

4.3 Measurements

4.3.1 Gain

1. Capture a screenshot of Vin and Vout with Vin = 1.0 Vpp sine wave at 1.0 KHz with appropriate on-screen measurements.
2. Calculate the gain, Av = $\frac{|Vout|}{|Vin|}$,
3. If either Vin or Vout appears clipped or distorted, reduce Vin until both Vin and Vout are nice clean looking sine waves, capture a new screenshot and recalculate the gain, Av.

4.3.2 Clipping

4. Slowly increase Vin until Vout begins to clip. Capture a screenshot and note whether the clipping starts on the positive or negative peaks.
5. Keep increasing Vin until the other polarity peaks of Vout begin to clip. Capture a screenshot.
6. Decrease Vin until Vout is again a clean-looking sine wave.

4.3.3 Bandwidth

As the input frequency is increased, holding the amplitude constant, the output sine wave will begin to drop. To find this frequency, keep increasing the frequency of Vin until Vout has fallen to about 70 percent of its amplitude at 1 kHz.

7. While the signal generator should remain nearly constant in amplitude, there will be a point where its output will also fall with increasing frequency. The objective of this measurement is to determine the frequency response of the amplifier, not the signal generator, so you will need to keep adjusting the signal generator output so its measured amplitude on the oscilloscope remains constant.
8. Capture a screenshot of the –3 dB bandwidth of this common emitter amplifier.

Keep the circuit set up as is; it will be used again in procedure 3 with only a minor modification.

4.4 Questions

1. Is the common emitter amplifier inverting or non-inverting?
2. When it clips on the upper peaks, what mode is the transistor in? Suggest a redesign of the amplifier to increase the upper clipping voltage.
3. When it clips on the bottom peaks, what mode is the transistor in? Suggest a redesign of the amplifier to decrease the lower clipping voltage.
4. When the input is capacitor coupled through C1, what is the DC voltage gain of this amplifier?
5. What function does the capacitor C1 serve?
6. Do your measured results agree with your simulation?

5 Common emitter amplifier with bypassed emitter resistor

In the common emitter amplifier with a bypassed emitter resister shown in figure 9 (same as figure 2), C2, a 10 µF electrolytic capacitor, is placed in parallel with emitter resistor, RE.

The emitter resistor RE is used in to aid in stabilizing the bias of transistor Q1, making it less sensitive to variations in the transistor β. However, it also has the effect of lowering the voltage gain of the amplifier.

The bias point only needs to be established for DC conditions, so if the amplifier is to be used for frequencies above DC, the emitter resistor can be bypassed by shunting it with a capacitor.

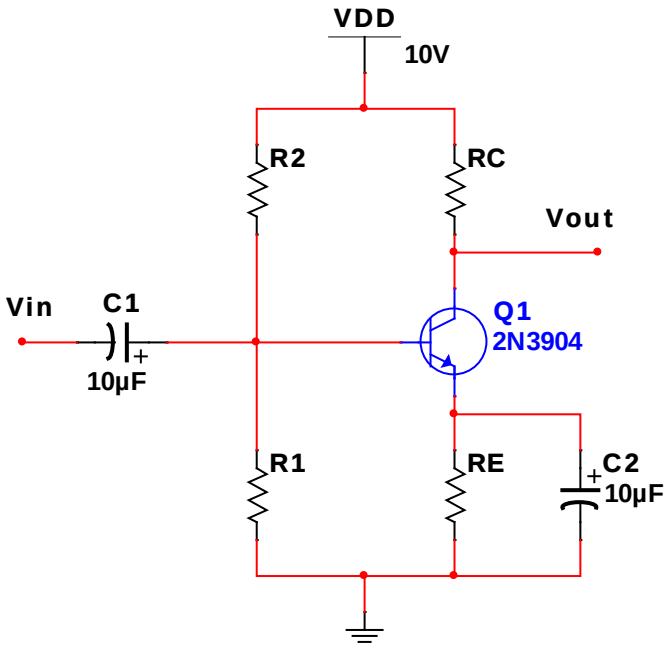

Figure 9. Common emitter with bypassed emitter resistor.

For DC, capacitor C2 is effectively an open-circuit, and RE stabilizes the bias point as before. At high frequencies, the impedance of capacitor C2 falls to the point where the emitter of Q1 is effectively grounded.

5.1 Simulation

Create a simulation using SPICE or Multisim of this circuit and copy and paste your schematic into your report.

5.1.1 Gain

1. Capture a screenshot of Vin and Vout from your simulation with Vin = 50 mVpp sine wave at 1.0 kHz with suitable cursors.
2. Calculate the voltage gain, Av = $\frac{|Vout|}{|Vin|}$, of this amplifier as the ratio of the amplitude of Vout to amplitude of Vin.

5.1.2 Clipping

3. Increase Vin until Vout begins clipping one peak or the other. Capture a screenshot with suitable cursors.
4. Continue increasing Vin until Vout begins clipping on both peaks. Capture a screenshot with suitable cursors.

5.1.3 Bandwidth

5. Reset Vin = 50.0 mVpp sine wave at 1.0 kHz.
6. Increase the frequency, holding the input amplitude constant, until Av has dropped by 3 dB. Capture a screenshot with suitable cursors.

5.2 Setup

Add C2 to the common emitter amplifier, bypassing the emitter resistor. Set Vin = 50 mVpp sine wave at 1.0 kHz. If the function generator won't go that low, you may need to use a voltage divider on its output.

5.3 Measurements

5.3.1 Gain

1. Adjust Vin so that Vout is as large as possible, but not yet clipping on either polarity peak and capture a screenshot with suitable on-screen measurements.
2. Calculate the voltage gain, Av = $\frac{|Vout|}{|Vin|}$.

5.3.2 Clipping

3. Increase Vin until Vout just begins to clip at either the negative or positive peak. Capture a screenshot with suitable on-screen measurements.
4. Continue increasing Vin until Vout begins clipping on the other peak. Capture a screenshot with suitable measurements.

5.3.3 Bandwidth

5. Reduce the amplitude of Vin until Vout is no longer clipped.
6. Holding the amplitude of Vin constant, increase the frequency of Vin until the amplitude of the output sine wave has fallen to about 70 percent of its initial value at 1 kHz. This will probably occur around 1 MHz. Capture a screenshot.

5.4 Questions

1. Is this amplifier inverting or non-inverting?
2. How do the clipping points compare to those of the common emitter amplifier without the emitter resistor bypass? Does the presence of the bypass capacitor affect the clipping levels?
3. Calculate the frequency at which the impedance of the bypass capacitor is equal to the resistance of RE. Above this frequency, capacitor C2 forms an effective bypass for RE.

4. What is the flat frequency response range for this amplifier?
5. How does the 3 dB bandwidth of the bypassed common emitter amplifier compare to the unbypassed case? Does the presence of the bypass capacitor have any effect on the high frequency characteristics?
6. Do your measured results agree with your simulation?

6 Common collector amplifier (emitter follower)

When the input signal is applied to the base terminal and the output signal taken from the emitter terminal as shown in figure 9 (same as figure 3), the collector terminal is thus common between the input and output ports, and the configuration is termed a common collector amplifier stage.

Since the voltage at the emitter essentially follows (tracks) the voltage at the base, this configuration is also called an emitter follower. Both names are synonymous and used equally.

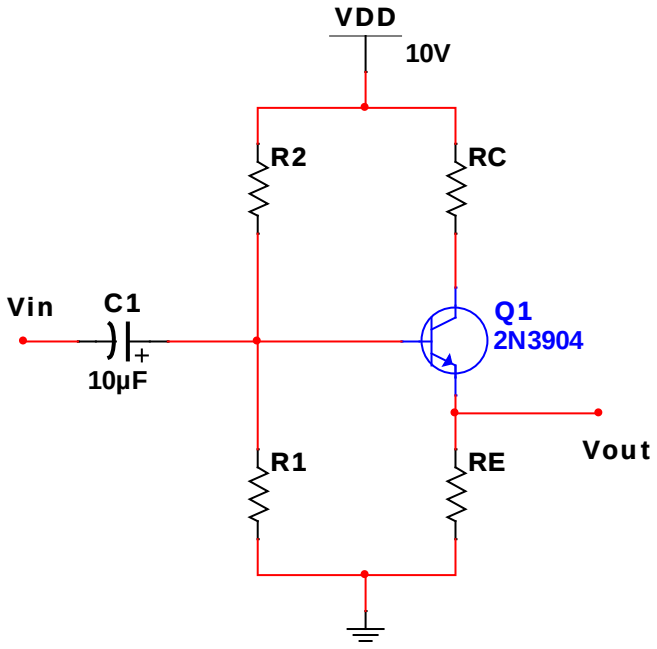

Figure 9. Common collector (emitter follower).

6.1 Simulation

Create a simulation using SPICE or Multisim of this circuit and copy and paste your schematic into your report.

6.1.1 Gain

1. Capture a screenshot of Vin and Vout from your simulation with Vin = 1.0 Vpp sine wave at 1.0 kHz with suitable cursors.
2. Calculate the voltage gain, Av = $\frac{|Vout|}{|Vin|}$, of this amplifier as the ratio of the amplitude of Vout to amplitude of Vin.

6.1.2 Clipping

3. Increase Vin until Vout begins clipping one peak or the other. Capture a screenshot with suitable cursors.

4. Continue increasing Vin until Vout begins clipping on both peaks. Capture a screenshot with suitable cursors.

6.1.3 Bandwidth

5. Reset Vin = 1.0 Vpp sine wave at 1.0 kHz.
6. Increase the frequency, holding the input amplitude constant, until Av has dropped by 3 dB. Capture a screenshot with suitable cursors.

6.2 Setup

Configure your circuit as shown in figure 9. The emitter resistor RE should not be bypassed. The output should be taken from the emitter.

Adjust the signal generator to produce a 1.0 Vpp 1.0 kHz sine wave.

6.3 Measurements

6.3.1 Gain

1. Adjust Vin so that Vout is as large as possible, but not yet clipping on either polarity peak and capture a screenshot with suitable on-screen measurements.
2. Calculate the voltage gain, Av = $\frac{|Vout|}{|Vin|}$.

6.3.2 Clipping

3. Increase Vin until Vout just begins to clip at either the negative or positive peak. Capture a screenshot with suitable on-screen measurements.
4. Continue increasing Vin until Vout begins clipping on the other peak or until you reach the maximum output of the signal generator. Capture a screenshot with suitable measurements.

6.3.3 Bandwidth

5. Reduce the amplitude of Vin until Vout is no longer clipped.
6. Holding the amplitude of Vin constant, increase the frequency of Vin until the amplitude of the output sine wave has fallen to about 70 percent of its initial value at 1 kHz. This will probably be over 10 MHz. Capture a screenshot.

6.4 Questions

1. Is the common collector amplifier inverting or non-inverting?

2. Since the voltage gain of this amplifier is actually less than unity, what is the usefulness of this amplifier?
3. Do your measured results agree with your simulation?

7 Common base amplifier

When the signal input is applied to the emitter terminal and the output drawn from the collector terminal as shown in figure 10 (same as figure 4) the base terminal is therefore common between the input and output ports, and the amplifier configuration is termed a common base.

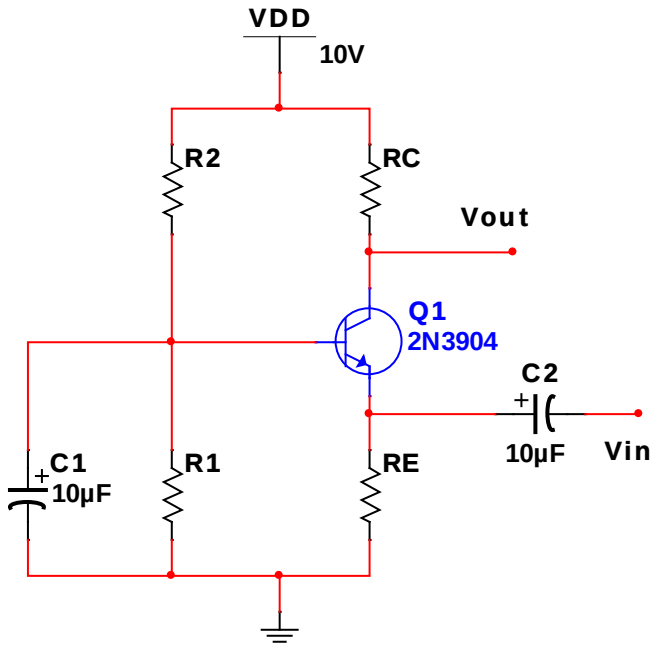

Figure 10. Common base.

7.1 Simulation

Create a simulation using SPICE or Multisim of this circuit and copy and paste your schematic into your report.

7.1.1 Gain

1. Capture a screenshot of Vin and Vout from your simulation with Vin = 100 mVpp sine wave at 1.0 kHz with suitable cursors.
2. Calculate the voltage gain, Av = $\frac{|Vout|}{|Vin|}$, of this amplifier as the ratio of the amplitude of Vout to amplitude of Vin.

7.1.2 Clipping

3. Increase Vin until Vout begins clipping one peak or the other. Capture a screenshot with suitable cursors.
4. Continue increasing Vin until Vout begins clipping on both peaks. Capture a screenshot with suitable cursors.

7.1.3 Bandwidth

5. Reset Vin = 100 mVpp sine wave at 1.0 kHz.
6. Increase the frequency, holding the input amplitude constant, until Av has dropped by 3 dB. Capture a screenshot with suitable cursors.

7.2 Setup

Configure your circuit as shown in figure 10. The input from the signal generator is applied to the emitter through C2. The base resistors R1 and R2 are bypassed by C1. Adjust Vin = 100 mVpp at 1.0 kHz sine wave.

7.3 Measurement

7.3.1 Gain

1. Adjust Vin so that Vout is as large as possible, but not yet clipping on either polarity peak and capture a screenshot with suitable on-screen measurements.
2. Calculate the voltage gain, Av = $\frac{|Vout|}{|Vin|}$.

7.3.2 Clipping

3. Increase Vin until Vout just begins to clip at either the negative or positive peak. Capture a screenshot with suitable on-screen measurements.
4. Continue increasing Vin until Vout begins clipping on the other peak. Capture a screenshot with suitable measurements.

7.3.3 Bandwidth

5. Reduce the amplitude of Vin until Vout is no longer clipped.
6. Holding the amplitude of Vin constant, increase the frequency of Vin until the amplitude of the output sine wave has fallen to about 70 percent of its initial value at 1 kHz. This will probably be over 1 MHz. Capture a screenshot.

7.4 Questions

1. Is the common base amplifier inverting or non-inverting?
2. Speculate on the effect of not bypassing the base resistors R1 and R2. If you don't have any ideas, go ahead and try this in the lab if you have time.
3. From the results of this lab experiment and those of experiment 1, explain why the base terminal of a BJT is never useful as an amplifier output.
4. From the results of this lab experiment and those of experiment 1, explain why the collector terminal of a BJT is never useful as an amplifier input.
5. Do your measured results agree with your simulation?